CHAPTER 2

Logic Gates

Contents

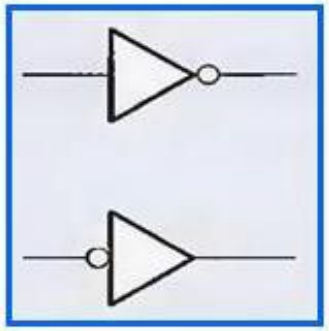
Boolean Variables & Truth Tables

LOGIC 0	LOGIC 1
False	True
Off	On
Low	High
No	Yes
Open Switch	Close Switch

A	B	X = A+B
0	0	0
0	1	1
1	0	1
1	1	1

Inverter

- **Inverter**
  - The inverter (NOT circuit) performs the operation called inversion or complementation.
  - The inverter changes one logic level to the opposite level.
  - In terms of bits, it changes a 1 to a 0 and a 0 to a 1.
  - Standard logic symbols for the inverter is,



Distinctive shape symbols with negation indicators

Inverter

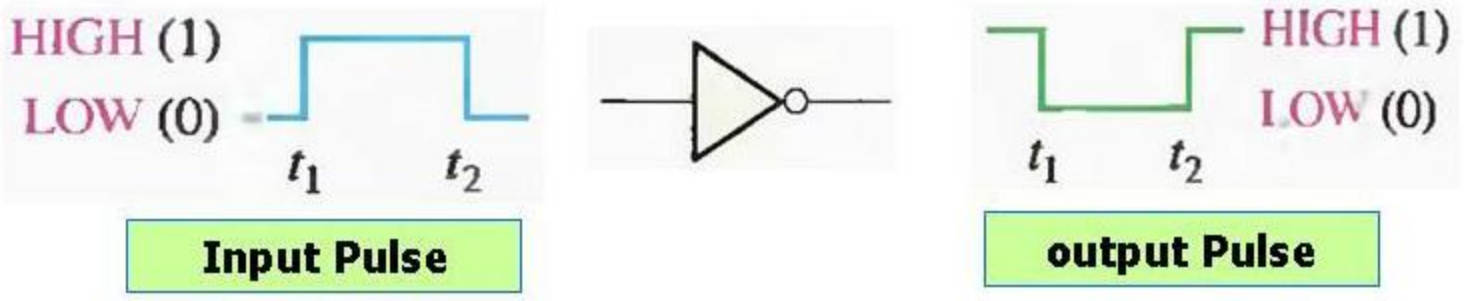
- **Inverter Truth Table**

INPUT	OUTPUT
LOW (0)	HIGH (1)
HIGH (1)	LOW (0)

  - A table such as this is called a truth table.
  - When a HIGH level is applied to an inverter input, a LOW level will appear on its output.

Inverter

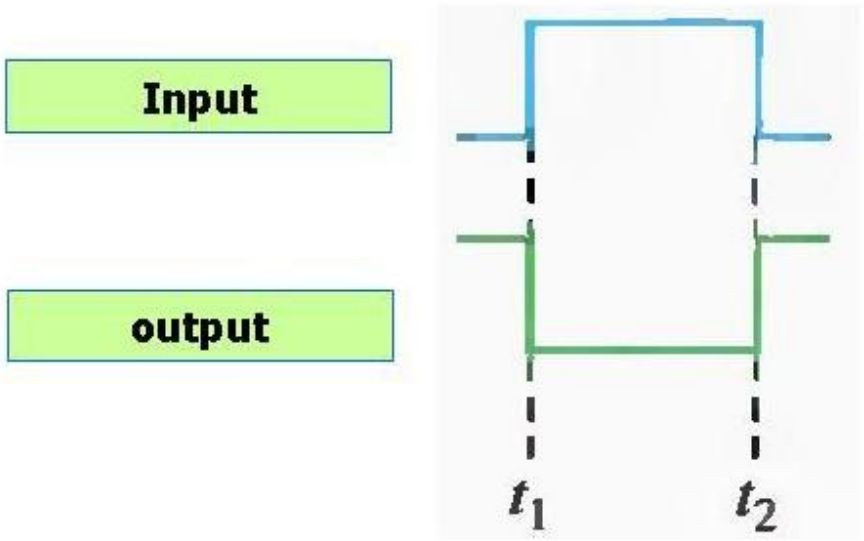
- **Inverter**
  - When the input is LOW, the output is HIGH and vice versa.
  - producing an inverted output pulse.
  - Standard logic symbols for the inverter is,



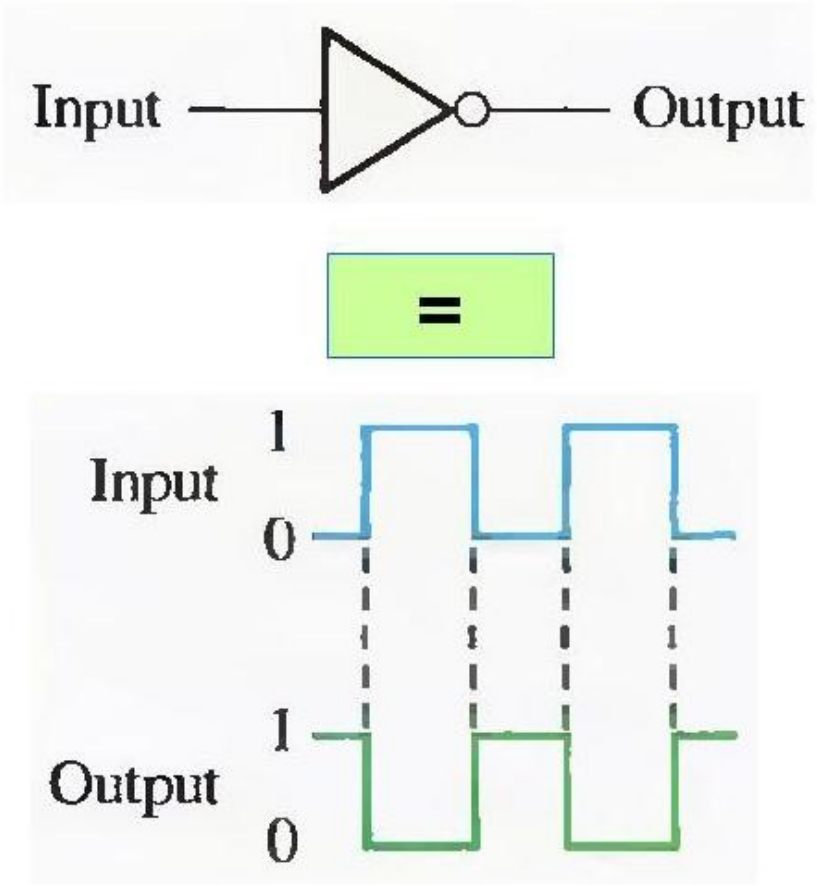
Inverter

Timing Diagram of Inverter

- timing diagram is basically a graph that accurately displays the relationship of two or more waveforms with respect to each other on a time basis. .

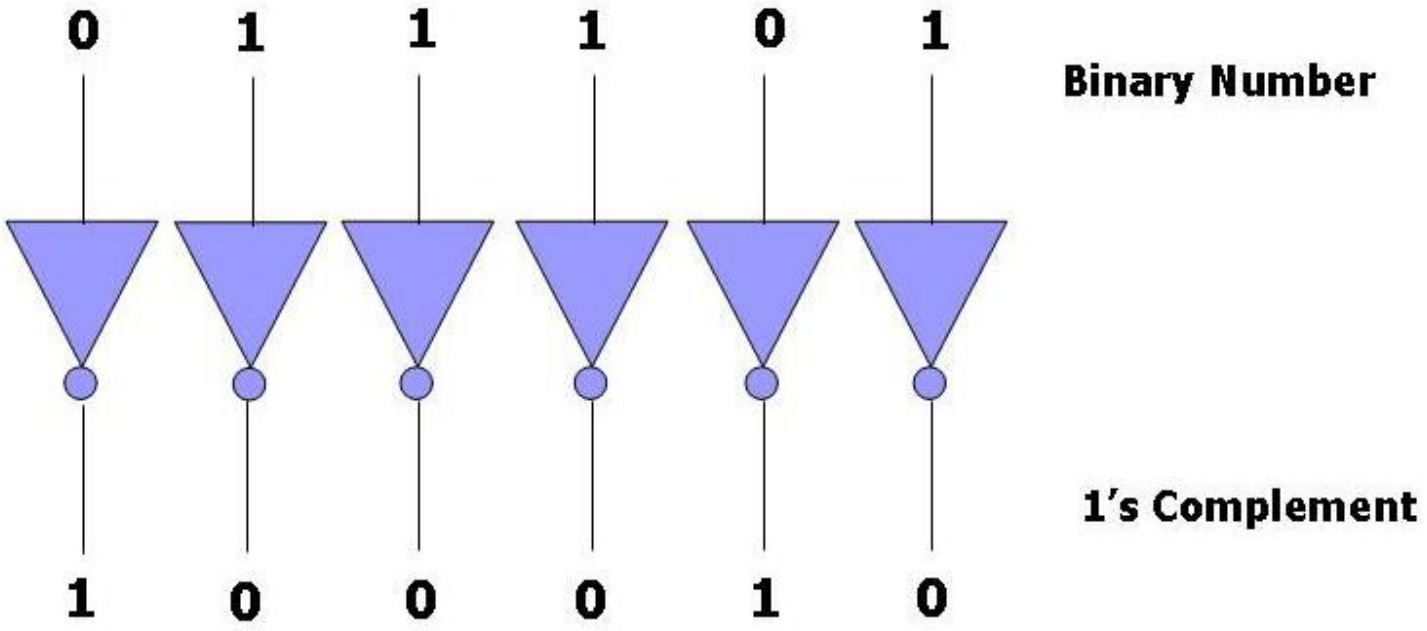


Timing Diagram Example



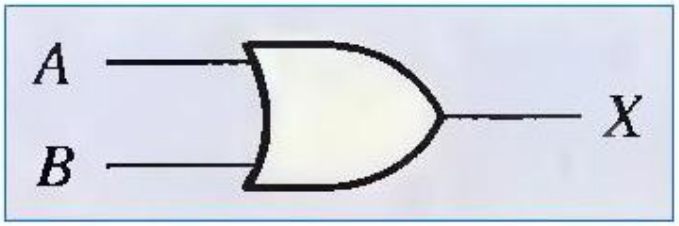
Inverter

Application of Inverter



OR Gate

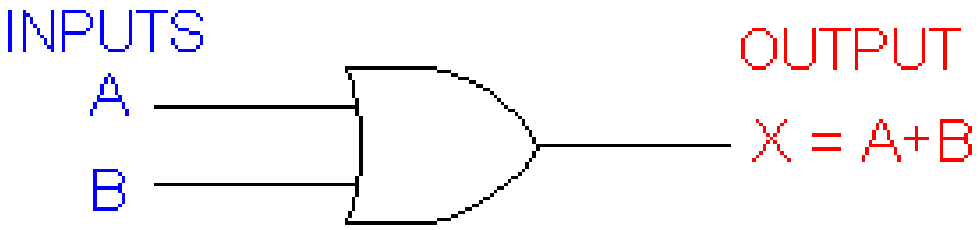
- An OR gate can have two or more inputs and performs what is known as logical addition.
- Standard logic symbols for the OR gate showing two input and single output.



- An OR gate can have any number of inputs greater than one.
- An OR gate produces a HIGH on the output when any of the inputs is HIGH.
- The output is LOW only when all of the inputs are LOW.

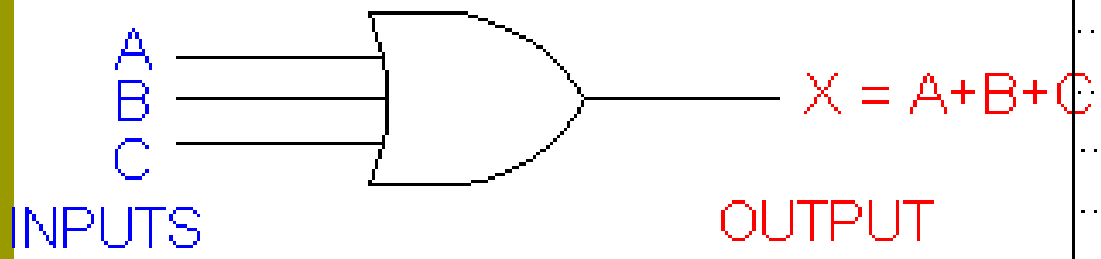
OR Operation

Two Inputs OR Gate



A	B	X = A+B
0	0	0
0	1	1
1	0	1
1	1	1

Three Inputs OR Gate



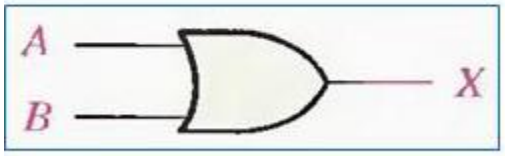
A	B	C	X = A+B+C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Logic Expression of OR

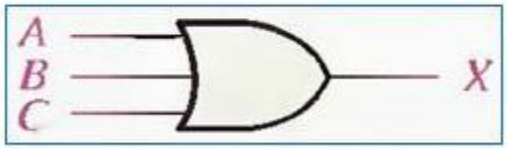
The operation of a 2-input OR gate can be expressed as follows: If one input variable is A, if the other input variable is B, and if the output variable is X, then the Boolean expression is

$$X=A+B$$

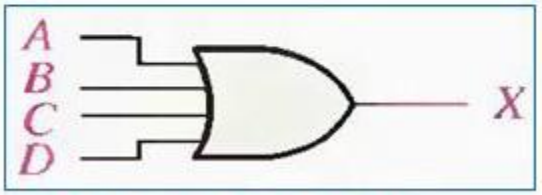
Boolean expressions for OR gates with two, three, and four inputs,



A+B=X

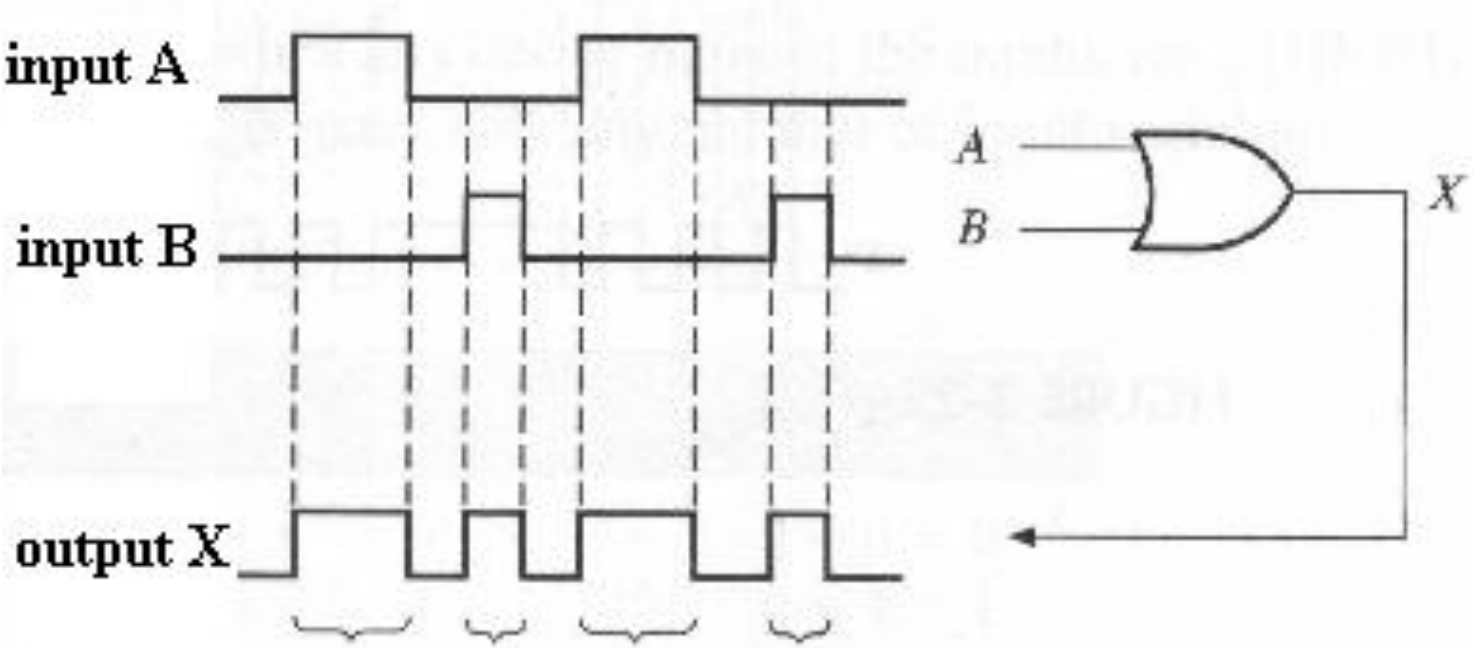


A+B+C=X



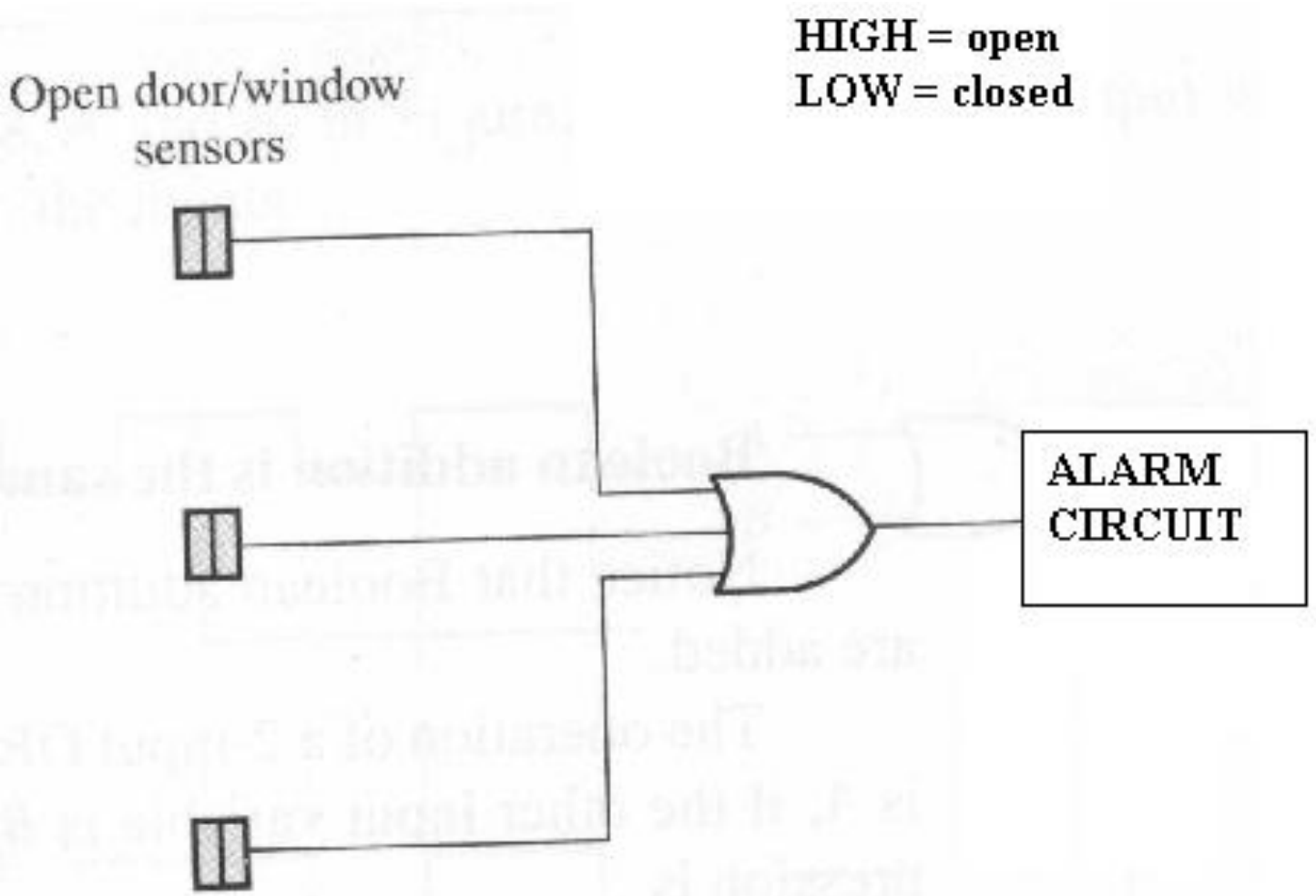
A+B+C+D=X

Timing Diagrams of OR gates



When either input or both inputs are HIGH, the output is HIGH

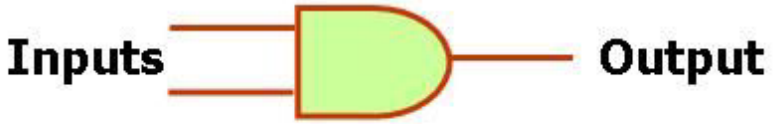
An application: Alarm System



AND Gate

AND Gate

- The AND gate is one of the basic gates that can be combined to form any logic function.
- An AND gate can have two or more inputs and performs what is known as logical multiplication.
- The term gate is used to describe a circuit that performs a basic logic operation.
- The AND gate is composed of two or more inputs and a single output.
- Standard logical symbol of AND gate is,

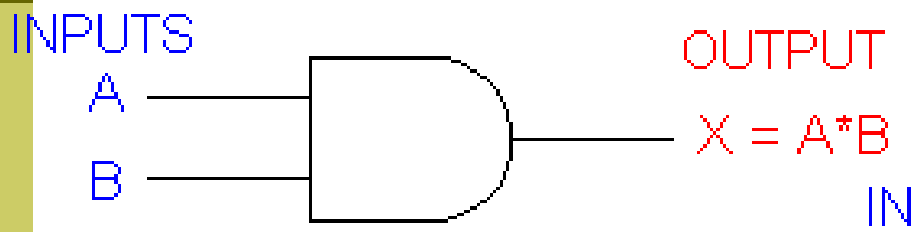


AND Gate

- **Operations of an AND Gate**
  - An AND gate produces a HIGH output only when all of the inputs are HIGH.
  - When any of the inputs is LOW, the output is LOW.
  - Therefore, the basic purpose of an AND gate is to determine when certain conditions are simultaneously true.

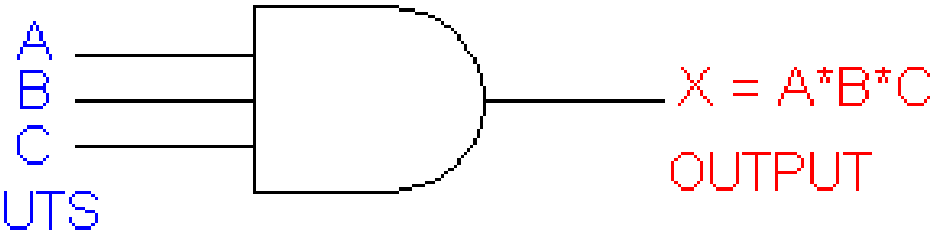
AND Operation

Two Inputs AND Gate



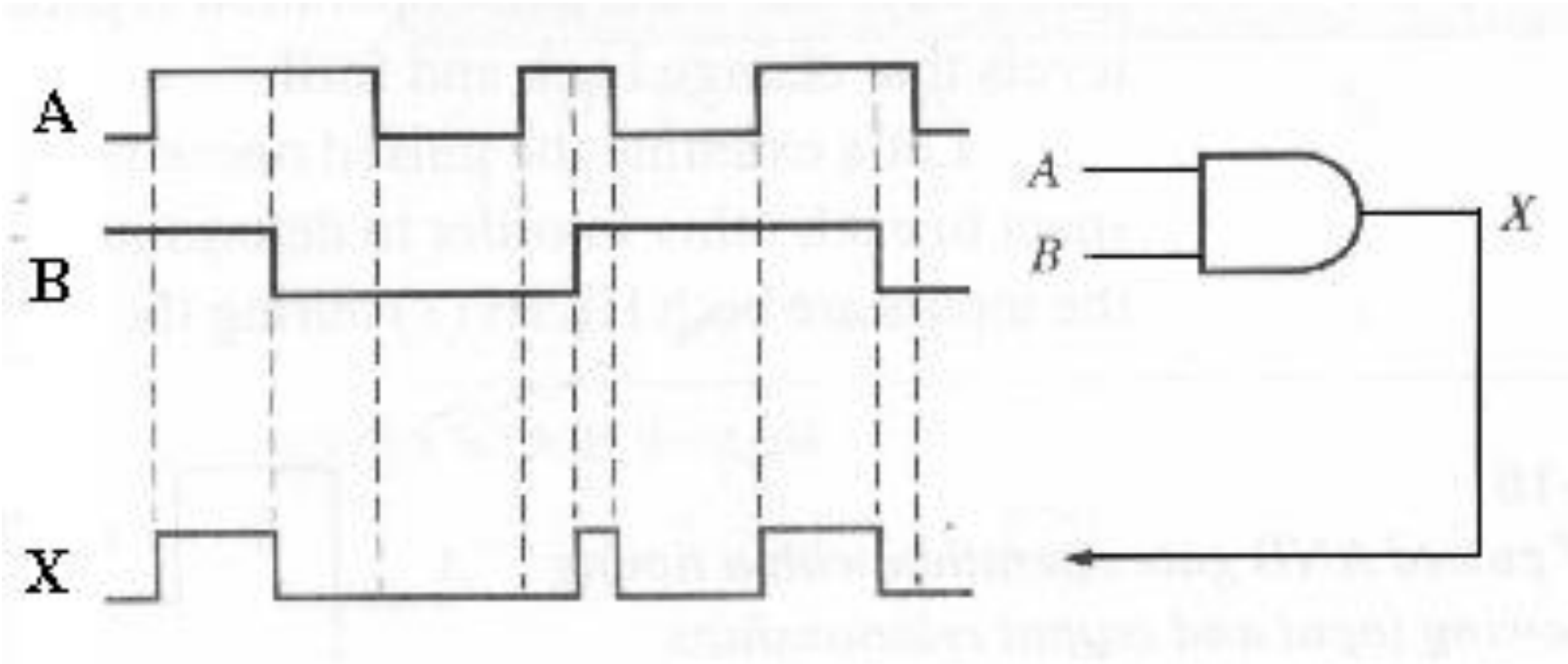
A	B	X = A*B
0	0	0
0	1	0
1	0	0
1	1	1

Three Inputs AND Gate



A	B	C	X = A*B*C
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

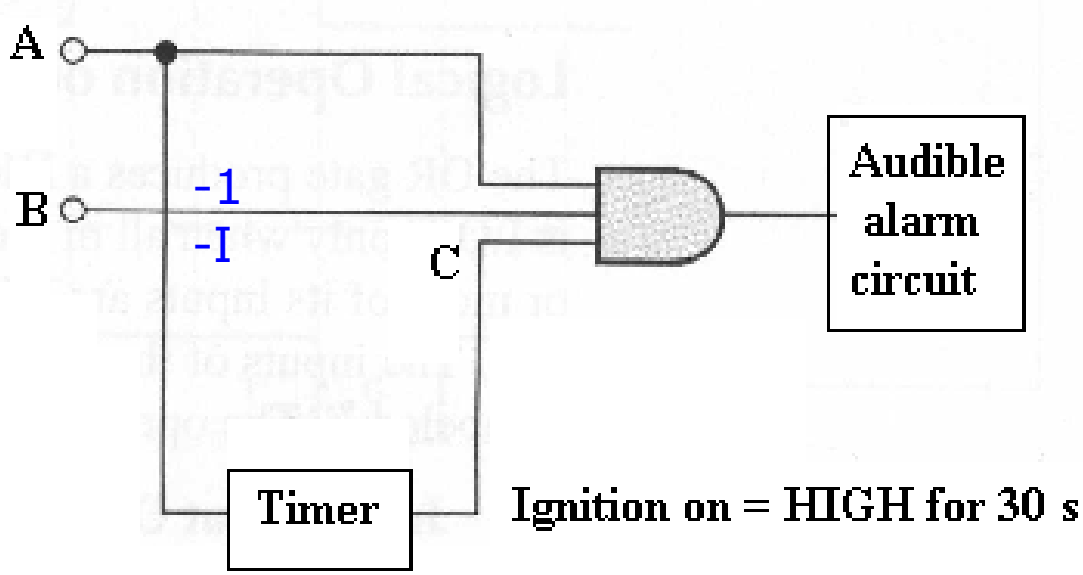
Timing Diagrams of AND gates



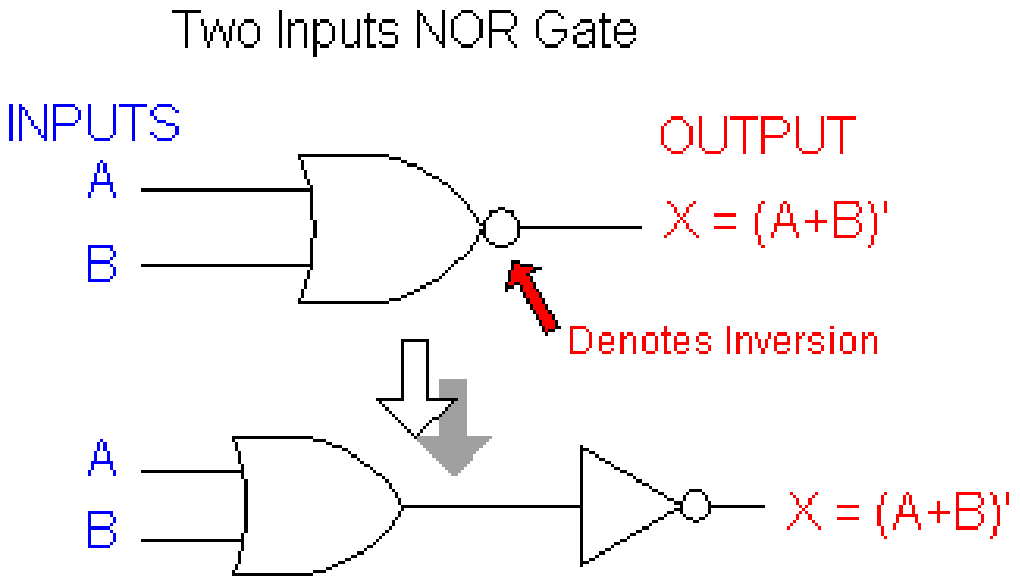
An application: A Seat Belt Alarm System

Ignition switch HIGH=ON LOW=OFF

Seat belt HIGH=Unbucked LOW=Bucked



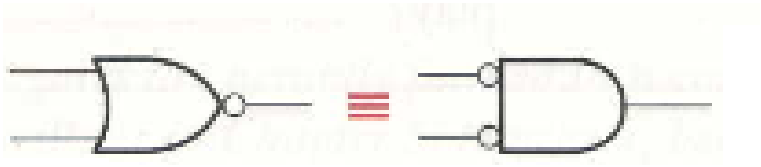
NOR Operation



INPUTS		OR	NOR
A	B	X = A+B	X= (A+B)'
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

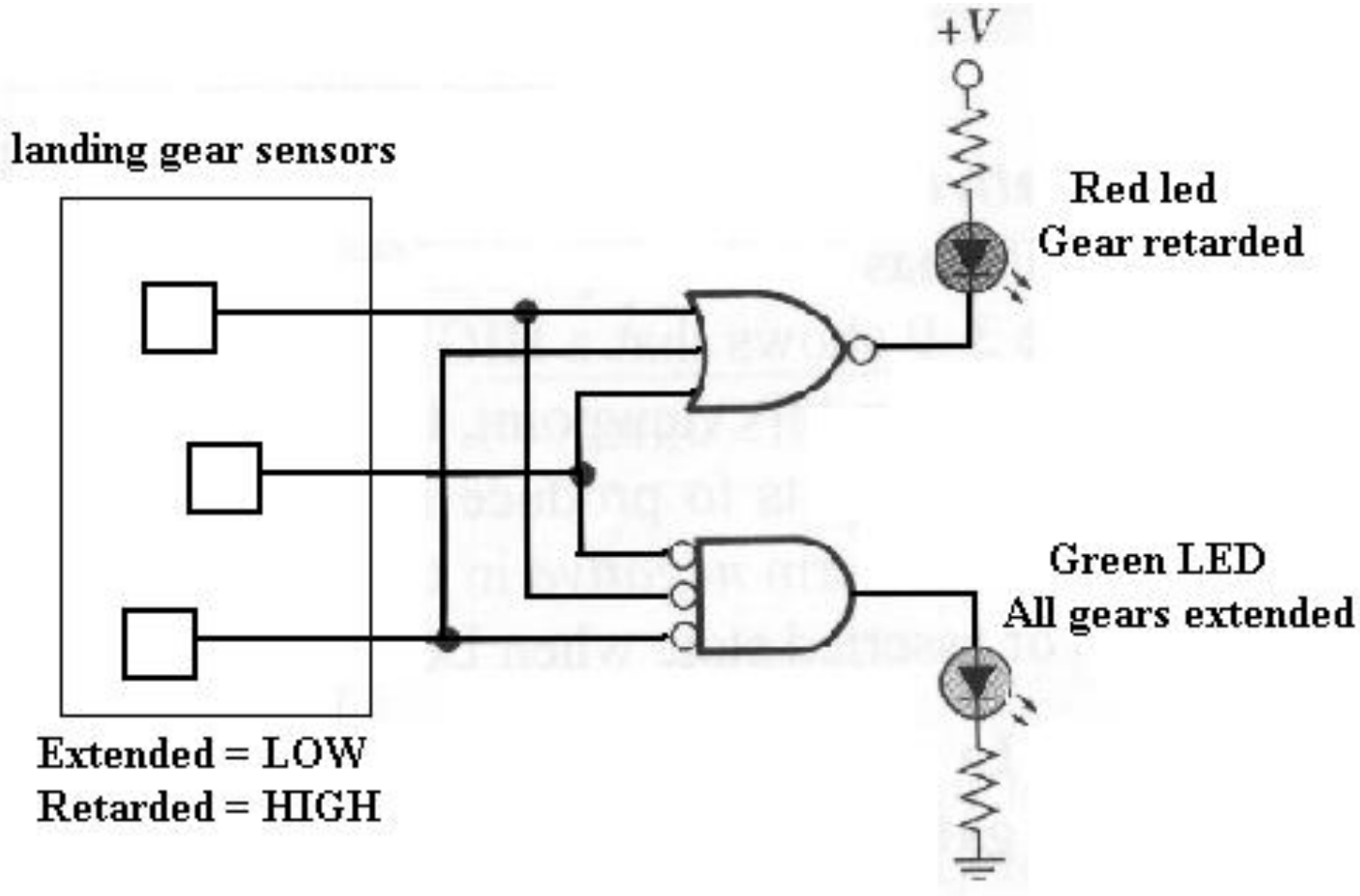
Negative AND equivalent of a NOR gate

Standard symbols representing the two equivalent operations of the NOR gate.



NOR Negative-AND

An application: An aircraft landing indicator



NAND Gate

The NAND gate is a popular logic element because it can be used as a universal gate.

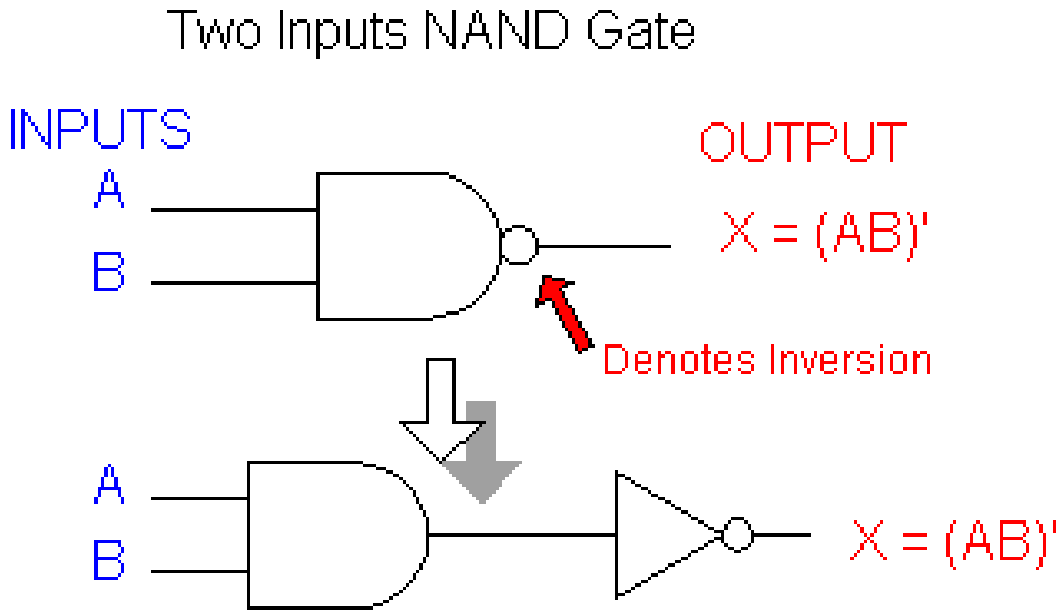
NAND gates can be used in combination to perform the AND, OR, and inverter operations.

The term NAND is a contraction of NOT-AND and implies an AND function with a Complemented (inverted) output.

The standard logic symbol for a 2-input

NAND gate and its equivalency to an AND gate followed by an inverter.

NAND Operation



INPUTS		AND	NAND
A	B	X = AB	X= (AB)'
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

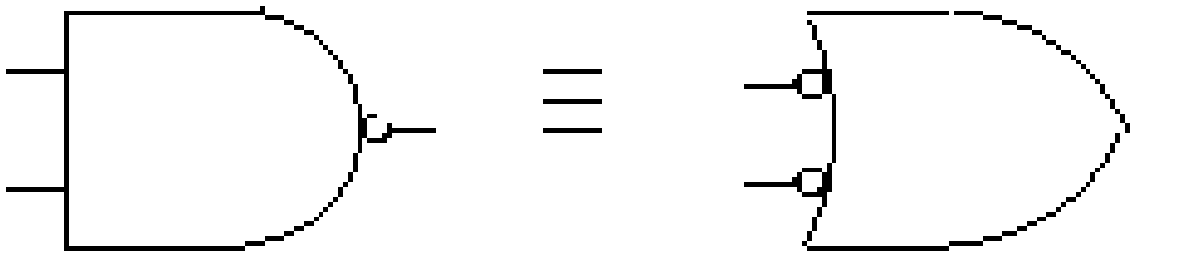
Logic Expression for NAND Gate

The Boolean expression for the output of a 2-input NAND gate is,

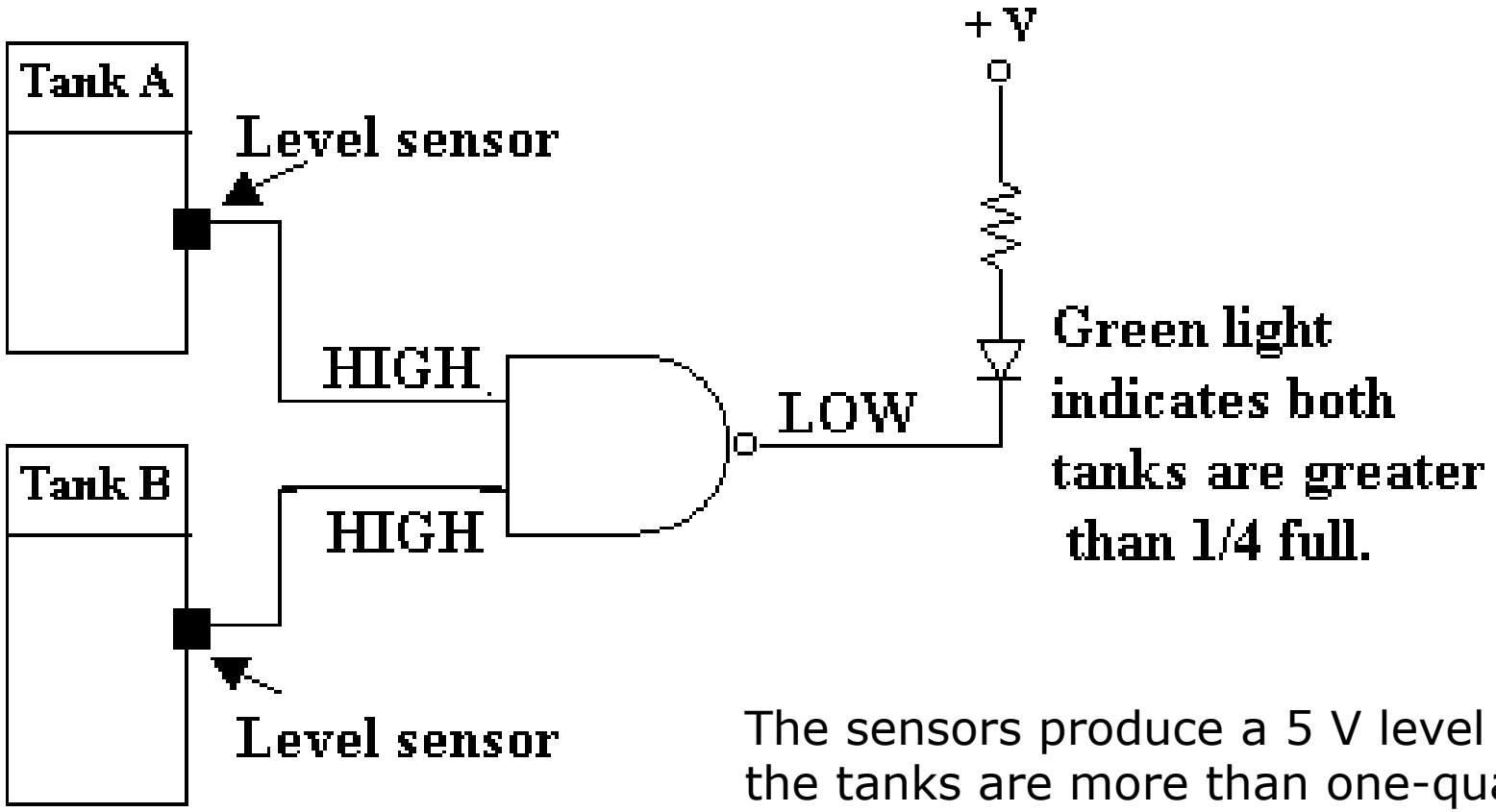
$$X = \overline{AB}$$

two input variables A and B, are first ANDed and then complemented, as indicated by the bar over the AND expression.

Negative OR Equivalent Operation of the NAND Gate

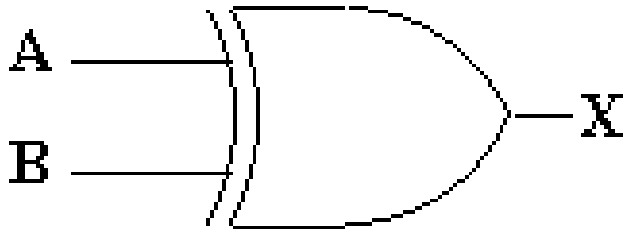


An application: A Manufacturing Plant Tank Indicator



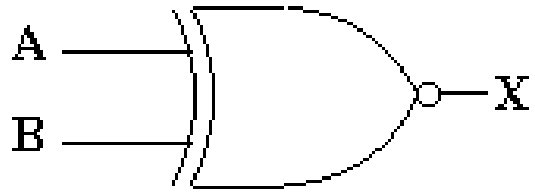
The sensors produce a 5 V level when the tanks are more than one-quarter full.

The Exclusive- OR Gate



Inputs		output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

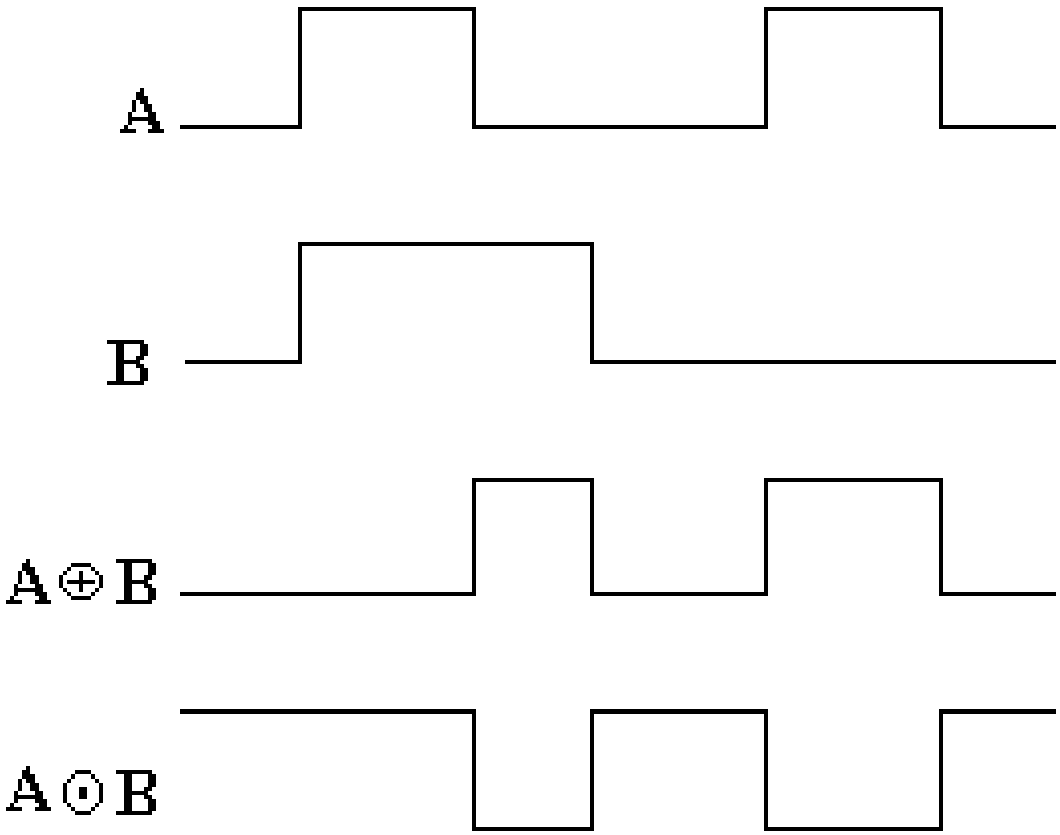
The Exclusive-NOR Gate



Inputs		output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

- equivalence 0
coincidence
X-NOR

Timing diagram



INTEGRATED CIRCUIT LOGIC FAMILIES

- Diode Logic (DL)
- Resistor-Transistor Logic (RTL)
- Diode-Transistor Logic (DTL)
- Transistor-Transistor Logic (TTL)
- Emitter-Coupled Logic (ECL)
- CMOS Logic

- **Fan-in**
  - The number of standard loads drawn by an input to ensure reliable operation. Most inputs have a fan-in of 1.
- **Fan-out**
  - The number of standard loads that can be reliably driven by an output, without causing the output voltage to shift out of its legal range of values.

Comparison of performance characteristics of CMOS, TTL and ECL logic gates.

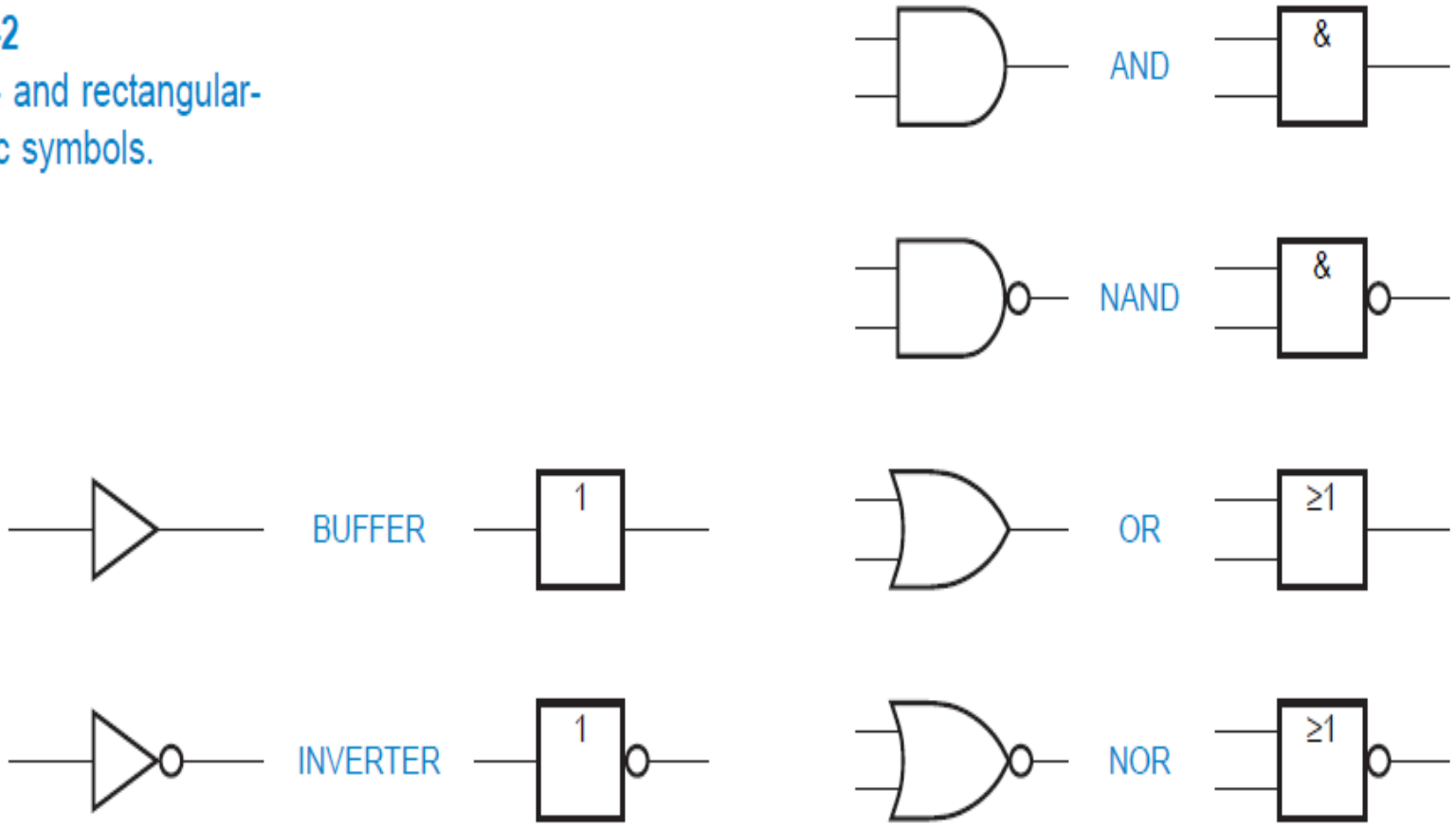
Technology	CMOS (silicon gate)	CMOS (metal gate)	TTL std	TTL LS	TTL S	TTL ALS	TTL AS	ECL
Device series	74HC	4000B	74	74LS	74S	74ALS	74AS	10KH
Power dissipation: Static		1 uW	10 mW	2 mW	19 mW	1 mW	8.5 mW	25 mW
At 100 kHz	0.17 mW	0.1 mW	10 mW	2 mW	19 mW	1 mW	8.5 mW	25 mW
Propagation delay time	8 ns	50 ns	10 ns	10 ns	3 ns	4 ns	1.5 ns	1 ns
Fan-out			10	20	20	20	40	

Std : standard LS: Low power Schottky S: Schottky

ALS: Advanced Low power Schottky AS: Advanced Schottky

IEEE symbols for logic gates

Figure A–2
Distinctive- and rectangular-shape logic symbols.



QUESTIONS?